REMARKS

The Official Action mailed February 11, 2003, has been received and its contents carefully noted. Filed concurrently herewith is a *Request for One Month Extension of Time*, which extends the shortened statutory period for response to June 11, 2003. Accordingly, Applicant respectfully submits that this response is being timely filed.

Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on May 30, 2000; October 4, 2000; September 26, 2001, and March 13, 2002. Applicant also notes the partial consideration of the Information Disclosure Statement filed on June 17, 1999. It is respectfully requested that the remaining references cited in this IDS be considered by the Examiner and an initialed Form 1449 returned evidencing such consideration. There does not appear to be any indication in the Official Action mailed December 27, 1999 as to why these references were not considered and it is respectfully submitted that the Examiner note any defects so that the same can be promptly remedied. Finally, it is noted that a further IDS was filed April 30, 2003 and review and consideration of the documents noted therein is requested.

Claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52-53, 58-60, 65, 71-73, 75-81 and 100-121 are now pending in the present application, of which claims 1-3, 8, 104, 107, 110, 113, 116 and 119 are independent. Claims 106, 109, 112, 115, 118, and 121 have been amended herewith. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 3 of the Official Action objects to claims 104, 107, 110, 113, 116, and 119 for a number of minor informalities. In response, applicant respectfully requests reconsideration. It is noted that the language objected to by the Examiner is included in issued U.S. Patent 6,355,940. In that this language is included in the issued '940 patent, it is believed to be unobjectionable and it is respectfully requested that the objections be withdrawn. Reconsideration is requested.

Paragraph 5 of the Official Action rejects claims 106, 109, 112, 115, 118, and 121 under 35 U.S.C. 112, first paragraph, asserting that each claim contains subject matter which was not described in the specification. In response, these claims have been amended and, as amended, are believed to be fully supported by the present specification. Favorable reconsideration is requested.

Paragraph 7 of the Official Action rejects claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52-53, 58-60, 65, 71-73, 75-81 and 100-103 as obvious based on the combination of U.S. Patent 5,403,772 to Zhang et al., U.S. Patent 5,233,447 to Kuribayashi et al., and U.S. Patent 5,173,792 to Matsueda.

As previously stressed, it is respectfully submitted that the Official Action has failed to establish a *prima facie* case of obviousness in that one of skill in the art would not have been motivated to combine the teachings of Zhang, Kuribayashi and Matsueda to achieve the present invention. Specifically, Matsueda discloses TFTs 100A and 100B provided at respective pixel portions of the display device, which is not related to the buffer circuit of the claimed invention. Particularly, it should be noted that Matsueda teaches two parallel-connected TFTs (100A and 100B) in Fig. 7 so that either one of the TFTs can be cut off if it is found to be defective (col. 13, line 57-col. 14, line 13).

In response to this argument, the Official Action asserts that Matsueda teaches that the reliability of a basic control element comprising two or more parallel-connected TFTs is better than that of a basic control element comprising a single TFT. The Official Action thus concludes that one of skill in the art would readily recognize that the reliability of the buffer circuit and/or other peripheral circuits in the active matrix type LC display device of Zhang would also be improved if the basic transistor in the buffer circuit and/or other peripheral circuits is formed of two or more parallel-connected TFTs.

Applicant respectfully disagrees. Matsueda is concerned about a specific problem unique to the pixel portion of an electrooptical display and is silent about the peripheral portion or buffer circuit. Neither Matsueda, nor the other prior art of record, discloses or suggest any problem with the prior art buffer circuit and thus one of skill in the art would not have been motivated to modify the buffer circuit to include parallel connected TFTs. Matsueda is silent concerning any problem with reliability in the driver circuit. While the Official Action asserts that such parallel connection would provide greater reliability and thus would be used in a buffer circuit and/or other peripheral circuits, there is no disclosure or suggestion that reliability in such circuits is a problem or that such parallel interconnection of TFTs could solve such problem if it even existed.

As previously noted, the Applicant has recognized a problem in prior art buffer circuits concerning excess heat caused by a large current in the buffer circuit as

described on page 19, lines 11-29. The present invention is based on a recognition of the problem caused by this excess heat in the buffer circuit, and the Applicants discovered that the problem could be solved when channel-forming regions of at least two transistors are separately provided in at least two separate islands respectively as shown in Fig. 3. Thus, Applicant's have recognized a specific problem that occurs in the buffer circuit and have presented a solution by the present invention.

The Official Action asserts that the fact that Applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. It is respectfully submitted, however, that there is no suggestion in the prior art and, absent the recognition of the problem discovered by Applicant, one of skill in the art would not be motivated to replace the buffer circuit of the prior art with the pixel circuit of Matsueda.

Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See MPEP 2143.01. It is respectfully submitted that the teachings of Matsueda are insufficient to teach or suggest to one of skill in the art that the buffer circuit should include parallel connected TFTs. At best, Matsueda teaches that the parallel TFTs could be used in a buffer circuit, not that they should not. See MPEP 2143.01, under the heading *FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH PRIMA FACIE OBVIOUSNESS*, wherein it is stated that "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. Reconsideration is requested.

The Official Action appears to assert that reliability is always a problem and that "Matsueda teaches that the reliability of a basic control element comprising two or more parallel-connected TFTs is better than that of a basic control element comprising a single TFT." It is respectfully submitted, however, that such characterization of

Matsueda is overly broad. Matsueda is not concerned with a "basic control element" but rather is concerned with a specific problem concerning defective display element circuits. Column 1, lines 6-14 make this clear, stating:

> The invention relates to electrooptical displays and more particularly to active matrix type electrooptical displays with redundant means to provide for substantially complete relief from defective circuits of display elements, also referred to in the art as picture elements or pixels. The built-in redundancy provides a means to correct for defective display element circuits in the fabricated display thereby increasing their manufacturing yield.

For all of the above reasons, it is respectfully submitted that one of skill in the art would not have been motivated to combine the references as asserted in the Official Action to achieve the present invention. A *prima* facie case of obviousness cannot be maintained and reconsideration is requested.

Paragraph 8 of the Official Action rejects claims 104-121 as obvious based on the combination of Zhang and Matsueda. For the same reasons as stressed above, it is respectfully submitted that the Official Action has failed to provide a sufficient basis to show that one of skill in the art would have been motivated to combine Zhang and Matsueda to achieve the present invention and thus a *prima facie* case of obviousness cannot be maintained. Favorable reconsideration is requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

106. (Amended) The display device according to claim 104, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.

109. (Amended) The display device according to claim 107, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.

112. (Amended) The display device according to claim 110, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.

115. (Amended) The display device according to claim 113, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.

118. (Amended) The display device according to claim 116, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.

121. (Amended) The display device according to claim 119, wherein the laser annealing is performed to [polycrystallize] crystallize an amorphous semiconductor layer in order to obtain a [polycrystalline] crystalline semiconductor layer.